查询NC7SZ74K8供应商

July 2001
Revised January 2005

# NC7SZ74
# TinyLogic® UHS D-Type Flip-Flop with Preset and Clear



## General Description

The NC7SZ74 is a single D-type CMOS Flip-Flop with preset and clear from Fairchild's Ultra High Speed Series of TinyLogic® in the space saving US8 package. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a very broad $V_{CC}$ operating range. The device is specified to operate over the 1.65V to 5.5V $V_{CC}$ range. The inputs and output are high impedance when $V_{CC}$ is 0V. Inputs tolerate voltages up to 7V independent of $V_{CC}$ operating voltage.

The signal level applied to the D input is transferred to the Q output during the positive going transition of the CLK pulse.

## Features

- Space saving US8 surface mount package
- MicroPak™ Pb-Free leadless package
- Ultra High Speed; $t_{PD}$ 2.6 ns Typ into 50 pF at 5V $V_{CC}$
- High Output Drive; ± 24 mA at 3V $V_{CC}$
- Broad $V_{CC}$ Operating Range; 1.65V to 5.5V
- Power down high impedance inputs/output
- Overvoltage tolerant inputs facilitate 5V to 3V translation
- Patented noise/EMI reduction circuitry implemented

## Ordering Code:

| Order Number | Package Number | Product Code Top Mark | Package Description | Supplied As |
|---|---|---|---|---|
| NC7SZ74K8X | MAB08A | SZ74 | 8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide | 3k Units on Tape and Reel |
| NC7SZ74L8X | MAC08A | N9 | Pb-Free 8-Lead MicroPak, 1.6 mm Wide | 5k Units on Tape and Reel |

Pb-Free package per JEDEC J-STD-020B.

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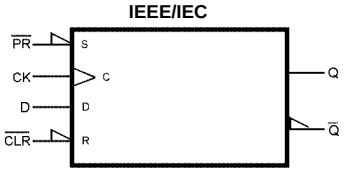
## Logic Symbol




## Pin Descriptions

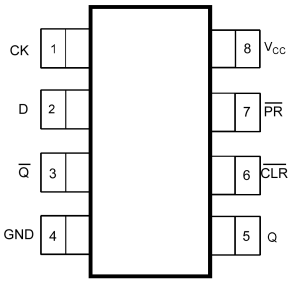
| Pin Names | Description |
|---|---|
| D | Data Input |
| CK | Clock Pulse Input |
| $\overline{CLR}$ | Direct Clear Input |
| Q, $\overline{Q}$ | Flip-Flop Output |
| $\overline{PR}$ | Direct Preset Input |

## Truth Table

| Inputs | | | | Outputs | | Function |
|---|---|---|---|---|---|---|
| $\overline{CLR}$ | $\overline{PR}$ | D | CK | Q | $\overline{Q}$ | |
| L | H | X | X | L | H | Clear |
| H | L | X | X | H | L | Preset |
| L | L | X | X | H | H | — |
| H | H | L | ↑ | L | H | — |
| H | H | H | ↑ | H | L | — |
| H | H | X | ↓ | $Q_n$ | $\overline{Q}_n$ | No Change |

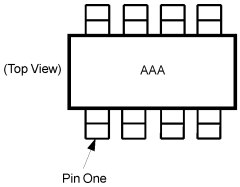
H = HIGH Logic Level
L = LOW Logic Level
$Q_n$ = No change in data
Z = High Impedance
X = Immaterial
↑ = Rising Edge
↓ = Falling edge

## Connection Diagrams




**(Top View)**

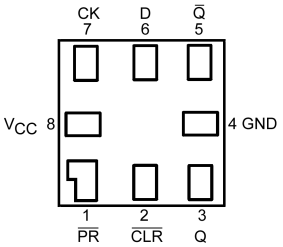
**Pin One Orientation Diagram**




AAA represents Product Code Top Mark - see ordering code

**Note:** Orientation of Top Mark determines Pin One location. Read the top product code mark left to right, Pin One is the lower left pin (see diagram).

**Pad Assignments for MicroPak**




**(Top Thru View)**

## Absolute Maximum Ratings (Note 1)

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.5V to +7.0V |
| DC Input Voltage ($V_{IN}$) | −0.5V to +7.0V |
| DC Output Voltage ($V_{OUT}$) | −0.5V to +7.0V |
| DC Input Diode Current ($I_{IK}$) | |
| $V_{IN}$ < 0V | −50 mA |
| DC Output Diode Current ($I_{OK}$) | |
| $V_{OUT}$ < 0V | −50 mA |
| DC Output ($I_{OUT}$) Source/Sink Current | ± 50 mA |
| DC $V_{CC}$/GND Current ($I_{CC}$/$I_{GND}$) | ± 50 mA |
| Storage Temperature Range ($T_{STG}$) | −65°C to +150°C |
| Junction Temperature under Bias ($T_J$) | 150°C |
| Junction Lead Temperature ($T_L$) | |
| (Soldering, 10 seconds) | 260°C |
| Power Dissipation ($P_D$) @ +85°C | 250 mW |

## Recommended Operating Conditions (Note 2)

| | |
|---|---|
| Power Supply | |
| Operating ($V_{CC}$) | 1.65V to 5.5V |
| Data Retention | 1.5V to 5.5V |
| Input Voltage ($V_{IN}$) | 0V to 5.5V |
| Output Voltage ($V_{OUT}$) | |
| Active State | 0V to $V_{CC}$ |
| 3-STATE | 0V to 5.5V |
| Input Rise and Fall Time ($t_r$, $t_f$) | |
| $V_{CC}$ = 1.8V, 2.5V ± 0.2V | 0 to 20 ns/V |
| $V_{CC}$ = 3.3V ± 0.3V | 0 to 10 ns/V |
| $V_{CC}$ = 5.5V ± 0.5V | 0 to 5 ns/V |
| Operating Temperature ($T_A$) | −40°C to +85°C |
| Thermal Resistance ($\theta_{JA}$) | 250° C/W |

**Note 1:** Absolute Maximum Ratings: are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 2:** Unused inputs must be held HIGH or LOW. They may not float.

## DC Electrical Characteristics

| Symbol | Parameter | $V_{CC}$ (V) | $T_A$ = +25°C | | | $T_A$ = −40°C to +85°C | | Units | Conditions | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | | | |
| $V_{IH}$ | HIGH Level Control Input Voltage | 1.65 to 1.95 | 0.75 $V_{CC}$ | | | 0.75 $V_{CC}$ | | V | | |
| | | 2.3 to 5.5 | 0.75 $V_{CC}$ | | | 0.7 $V_{CC}$ | | | | |
| $V_{IL}$ | LOW Level Control Input Voltage | 1.65 to 1.95 | | | 0.25 $V_{CC}$ | | 0.25 $V_{CC}$ | V | | |
| | | 2.3 to 5.5 | | | 0.3 $V_{CC}$ | | 0.3 $V_{CC}$ | | | |
| $V_{OH}$ | HIGH Level Control Output Voltage | 1.65 | 1.55 | 1.65 | | 1.55 | | | | |
| | | 2.3 | 2.2 | 2.3 | | 2.2 | | | | $I_{OH}$ = −100 µA |
| | | 3.0 | 2.9 | 3.0 | | 2.9 | | | | |
| | | 4.5 | 4.4 | 4.5 | | 4.4 | | | | |
| | | 1.65 | 1.29 | 1.52 | | 1.29 | | V | $V_{IN}$ = $V_{IH}$ | $I_{OH}$ = −4 mA |
| | | 2.3 | 1.9 | 2.15 | | 1.9 | | | | $I_{OH}$ = −8 mA |
| | | 3.0 | 2.4 | 2.8 | | 2.4 | | | | $I_{OH}$ = −16 mA |
| | | 3.0 | 2.3 | 2.68 | | 2.3 | | | | $I_{OH}$ = −24 mA |
| | | 4.5 | 3.8 | 4.2 | | 3.8 | | | | $I_{OH}$ = −32 mA |
| $V_{OL}$ | LOW Level Control Output Voltage | 1.65 | | | 0.1 | | 0.1 | | | |
| | | 2.3 | | | 0.1 | | 0.1 | | | $I_{OL}$ = 100 µA |
| | | 3.0 | | | 0.1 | | 0.1 | | | |
| | | 4.5 | | | 0.1 | | 0.1 | | | |
| | | 1.65 | | 0.08 | 0.24 | | 0.24 | V | $V_{IN}$ = $V_{IH}$ | $I_{OL}$ = 4 mA |
| | | 2.3 | | 0.10 | 0.3 | | 0.3 | | | $I_{OL}$ = 8 mA |
| | | 3.0 | | 0.15 | 0.4 | | 0.4 | | | $I_{OL}$ = 16 mA |
| | | 3.0 | | 0.22 | 0.55 | | 0.55 | | | $I_{OL}$ = 24 mA |
| | | 4.5 | | 0.22 | 0.55 | | 0.55 | | | $I_{OL}$ = 32 mA |
| $I_{IN}$ | Input Leakage Current | 0 to 5.5 | | | ±0.1 | | ±1.0 | µA | 0 ≤ $V_{IN}$ ≤ 5.5V | |
| $I_{OFF}$ | Power Off Leakage Current | 0.0 | | | 1.0 | | 10 | µA | $V_{IN}$ or $V_{OUT}$ = 5.5V | |
| $I_{CC}$ | Quiescent Supply Current | 1.65 to 5.5 | | | 1.0 | | 10.0 | µA | $V_{IN}$ = 5.5V, GND | |

## AC Electrical Characteristics

| Symbol | Parameter | $V_{CC}$ (V) | $T_A = +25°C$ | | | $T_A = -40°C$ to $+85°C$ | | Units | Conditions | Figure Number |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | | | |
| $f_{MAX}$ | Maximum Clock Frequency | 1.8 ± 0.15 | 75 | | | 75 | | MHz | $C_L$ = 15 pF, $R_D$ = 1 MΩ, $S_1$ = Open | Figures 1, 5 |
| | | 2.5 ± 0.2 | 150 | | | 150 | | | | |
| | | 3.3 ± 0.3 | 200 | | | 200 | | | | |
| | | 5.0 ± 0.5 | 250 | | | 250 | | | | |
| | | 3.3 ± 0.3 | 175 | | | 175 | | | $C_L$ = 50 pF, $R_D$ = 500Ω, $S_1$ = Open | |
| | | 5.0 ± 0.5 | 200 | | | 200 | | | | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay CK to Q, $\overline{Q}$ | 1.8 ± 0.15 | 2.5 | 6.5 | 12.5 | 2.5 | 13.0 | ns | $C_L$ = 15 pF, $R_D$ = 1 MΩ, $S_1$ = Open | Figures 1, 3 |
| | | 2.5 ± 0.2 | 1.5 | 3.8 | 7.5 | 1.5 | 8.0 | | | |
| | | 3.3 ± 0.3 | 1.0 | 2.8 | 6.5 | 1.0 | 7.0 | | | |
| | | 5.0 ± 0.5 | 0.8 | 2.2 | 4.5 | 0.8 | 5.0 | | | |
| | | 3.3 ± 0.3 | 1.0 | 3.4 | 7.0 | 1.0 | 7.5 | | $C_L$ = 50 pF, $R_D$ = 500 Ω, $S_1$ = Open | |
| | | 5.0 ± 0.5 | 1.0 | 2.6 | 5.0 | 1.0 | 5.5 | | | |
| $t_{PLH}$ $t_{PHL}$ | Propagation Delay $\overline{CLR}$, $\overline{PR}$, to Q, $\overline{Q}$ | 1.8 ± 0.15 | 2.5 | 6.5 | 14.0 | 2.5 | 14.5 | ns | $C_L$ = 15 pF, $R_D$ = 1 MΩ, $S_1$ = Open | Figures 1, 3 |
| | | 2.5 ± 0.2 | 1.5 | 3.8 | 9.0 | 1.5 | 9.5 | | | |
| | | 3.3 ± 0.3 | 1.0 | 2.8 | 6.5 | 1.0 | 7.0 | | | |
| | | 5.0 ± 0.5 | 0.8 | 2.2 | 5.0 | 0.8 | 5.5 | | | |
| | | 3.3 ± 0.3 | 1.0 | 3.4 | 7.0 | 1.0 | 7.5 | | $C_L$ = 50 pF, $R_D$ = 500 Ω, $S_1$ = Open | |
| | | 5.0 ± 0.5 | 1.0 | 2.6 | 5.0 | 1.0 | 5.5 | | | |
| $t_S$ | Setup Time, CK to D | 1.8 ± 0.15 | 6.5 | | | 6.5 | | ns | $C_L$ = 15 pF, $R_D$ = 1 MΩ, $S_1$ = Open | Figures 1, 4 |
| | | 2.5 ± 0.2 | 3.5 | | | 3.5 | | | | |
| | | 3.3 ± 0.3 | 2.0 | | | 2.0 | | | | |
| | | 5.0 ± 0.5 | 1.5 | | | 1.5 | | | | |
| | | 3.3 ± 0.3 | 2.0 | | | 2.0 | | | $C_L$ = 50 pF, $R_D$ = 500 Ω, $S_1$ = Open | |
| | | 5.0 ± 0.5 | 1.5 | | | 1.5 | | | | |
| $t_H$ | Hold Time, CK to D | 1.8 ± 0.15 | 0.5 | | | 0.5 | | ns | $C_L$ = 15 pF, $R_D$ = 1 MΩ, $S_1$ = Open | Figures 1, 4 |
| | | 2.5 ± 0.2 | 0.5 | | | 0.5 | | | | |
| | | 3.3 ± 0.3 | 0.5 | | | 0.5 | | | | |
| | | 5.0 ± 0.5 | 0.5 | | | 0.5 | | | | |
| | | 3.3 ± 0.3 | 0.5 | | | 0.5 | | | $C_L$ = 50 pF, $R_D$ = 500 Ω, $S_1$ = Open | |
| | | 5.0 ± 0.5 | 0.5 | | | 0.5 | | | | |
| $t_W$ | Pulse Width, CK, $\overline{PR}$, $\overline{CLR}$ | 1.8 ± 0.15 | 6.0 | | | 6.0 | | ns | $C_L$ = 15 pF, $R_D$ = 1 MΩ, $S_1$ = Open | Figures 1, 5 |
| | | 2.5 ± 0.2 | 4.0 | | | 4.0 | | | | |
| | | 3.3 ± 0.3 | 3.0 | | | 3.0 | | | | |
| | | 5.0 ± 0.5 | 2.0 | | | 2.0 | | | | |
| | | 3.3 ± 0.3 | 3.0 | | | 3.0 | | | CL = 50 pF, $R_D$ = 500 Ω, $S_1$ = Open | |
| | | 5.0 ± 0.5 | 2.0 | | | 2.0 | | | | |
| $t_{REC}$ | Recover Time $\overline{CLR}$, $\overline{PR}$ to CK | 1.8 ± 0.15 | 8.0 | | | 8.0 | | ns | $C_L$ = 15 pF, $R_D$ = 1 MΩ, $S_1$ = Open | Figures 1, 4 |
| | | 2.5 ± 0.2 | 4.5 | | | 4.5 | | | | |
| | | 3.3 ± 0.3 | 3.0 | | | 3.0 | | | | |
| | | 5.0 ± 0.5 | 3.0 | | | 3.0 | | | | |
| | | 3.3 ± 0.3 | 3.0 | | | 3.0 | | | $C_L$ = 50 pF, $R_D$ = 500 Ω, $S_1$ = Open | |
| | | 5.0 ± 0.5 | 3.0 | | | 3.0 | | | | |

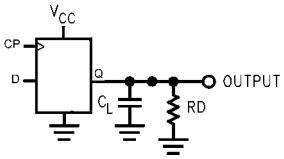
## Capacitance (Note 3)

| Symbol | Parameter | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 3 | | pF | $V_{CC}$ = 0V |
| $C_{OUT}$ | Output Capacitance | 4 | | pF | $V_{CC}$ = 0V |
| $C_{PD}$ | Power Dissipation Capacitance (Note 4) | 10 | | pF | $V_{CC}$ = 3.3V |
| | | 12 | | | $V_{CC}$ = 5.0V |

**Note 3:** $T_A$ = +25C, f = 1MHz.

**Note 4:** $C_{PD}$ is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption ($I_{CCD}$) at no output loading and operating at 50% duty cycle. (See Figure 2) $C_{PD}$ is related to $I_{CCD}$ dynamic operating current by the expression: $I_{CCD} = (C_{PD})\ (V_{CC})\ (f_{IN}) + (I_{CC}static)$.

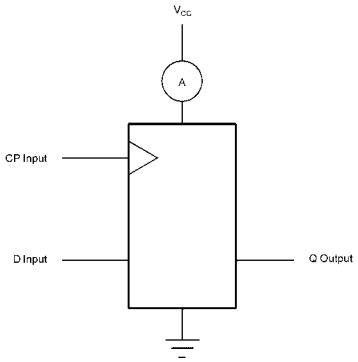
## AC Loading and Waveforms




$C_L$ includes load and stray capacitance

Input PRR = 1.0 MHz; $t_w$ = 500 ns

**FIGURE 1. AC Test Circuit**




CP Input = AC Waveform; $t_r = t_f$ = 2.5 ns;

CP Input PRR = 10 MHz; Duty Cycle = 50%

D Input PRR = 5MHz; Duty Cycle = 50%

**FIGURE 2. $I_{CCD}$ Test Circuit**

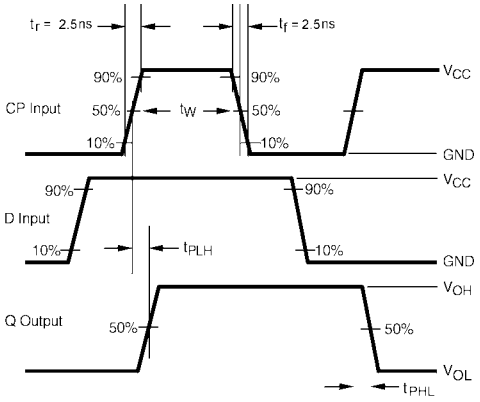



**FIGURE 3. AC Waveforms**

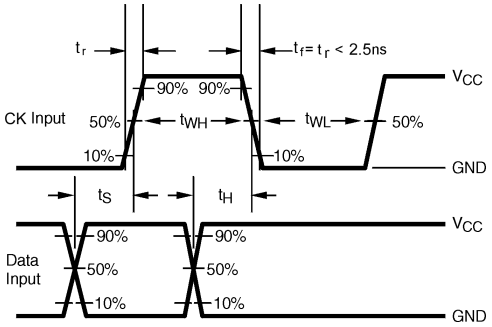



**FIGURE 4. AC Waveforms**

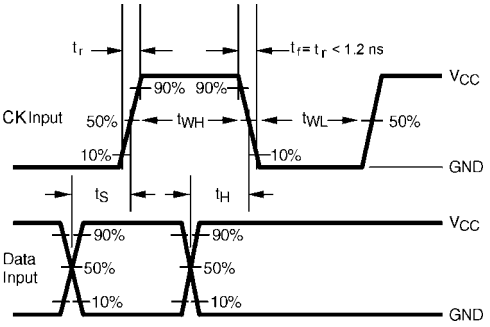


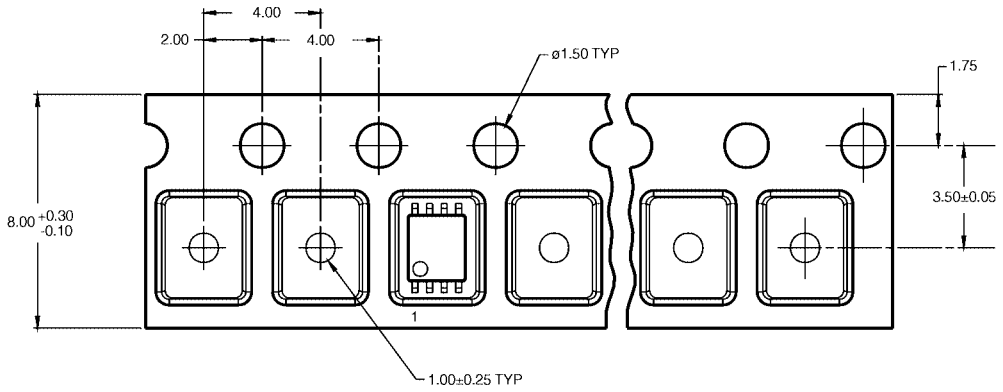

**FIGURE 5. AC Waveforms**

## Tape and Reel Specification

**TAPE FORMAT for US8**

| Package Designator | Tape Section | Number Cavities | Cavity Status | Cover Tape Status |
|---|---|---|---|---|
| K8X | Leader (Start End) | 125 (typ) | Empty | Sealed |
| | Carrier | 3000 | Filled | Sealed |
| | Trailer (Hub End) | 75 (typ) | Empty | Sealed |

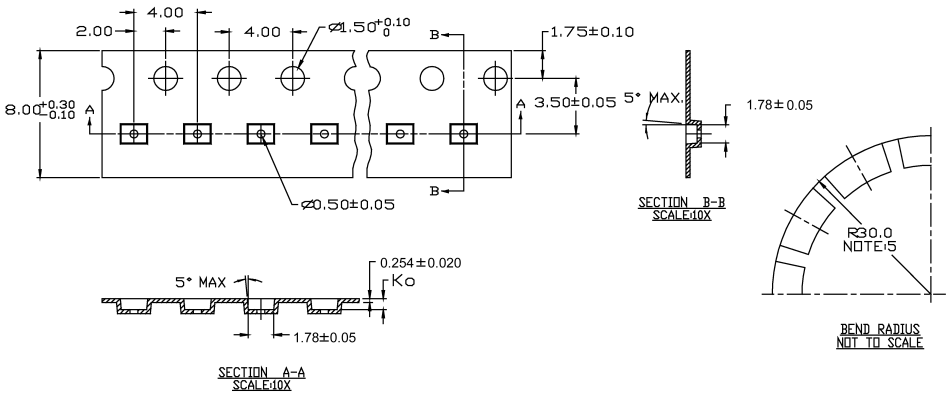
**TAPE DIMENSIONS** inches (millimeters)




**TAPE FORMAT for MicroPak**

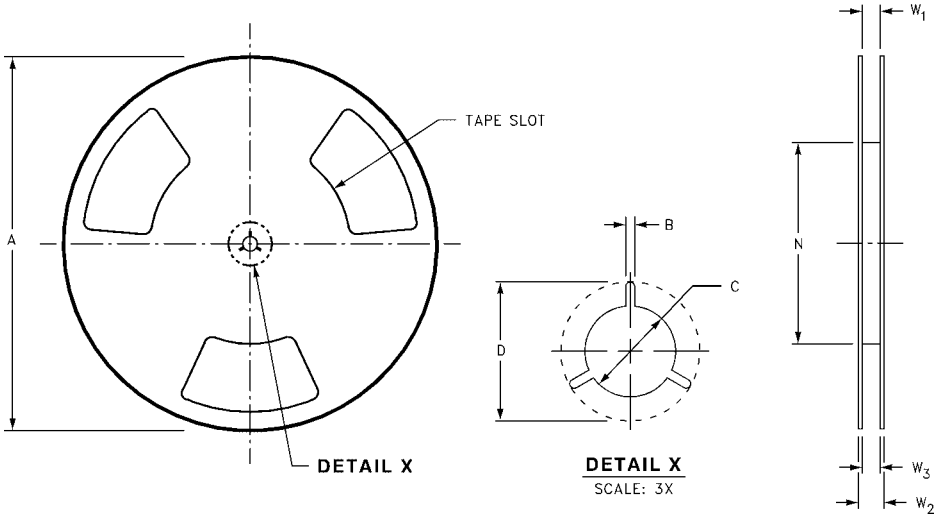
| Package Designator | Tape Section | Number Cavities | Cavity Status | Cover Tape Status |
|---|---|---|---|---|
| L8X | Leader (Start End) | 125 (typ) | Empty | Sealed |
| | Carrier | 3000 | Filled | Sealed |
| | Trailer (Hub End) | 75 (typ) | Empty | Sealed |

**TAPE DIMENSIONS** inches (millimeters)



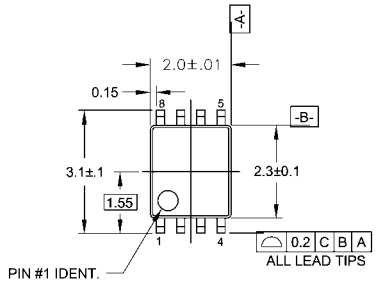
## Tape and Reel Specification (Continued)

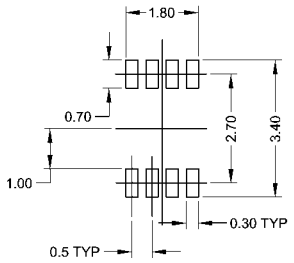
**REEL DIMENSIONS** inches (millimeters)



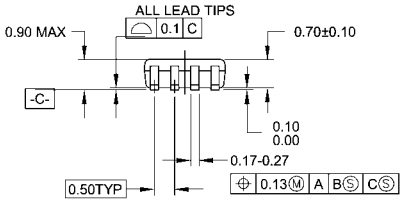

| Tape Size | A | B | C | D | N | W1 | W2 | W3 |
|---|---|---|---|---|---|---|---|---|
| 8 mm | 7.0<br>(177.8) | 0.059<br>(1.50) | 0.512<br>(13.00) | 0.795<br>(20.20) | 2.165<br>(55.00) | 0.331 + 0.059/–0.000<br>(8.40 + 1.50/–0.00) | 0.567<br>(14.40) | W1 + 0.078/–0.039<br>(W1 + 2.00/–1.00) |

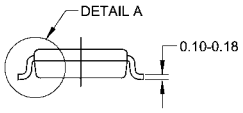
## Physical Dimensions inches (millimeters) unless otherwise noted

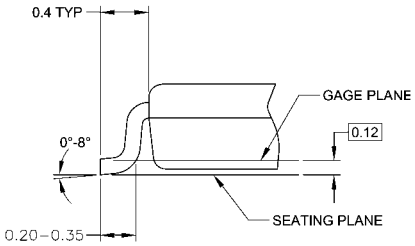



LAND PATTERN RECOMMENDATION




DETAIL A

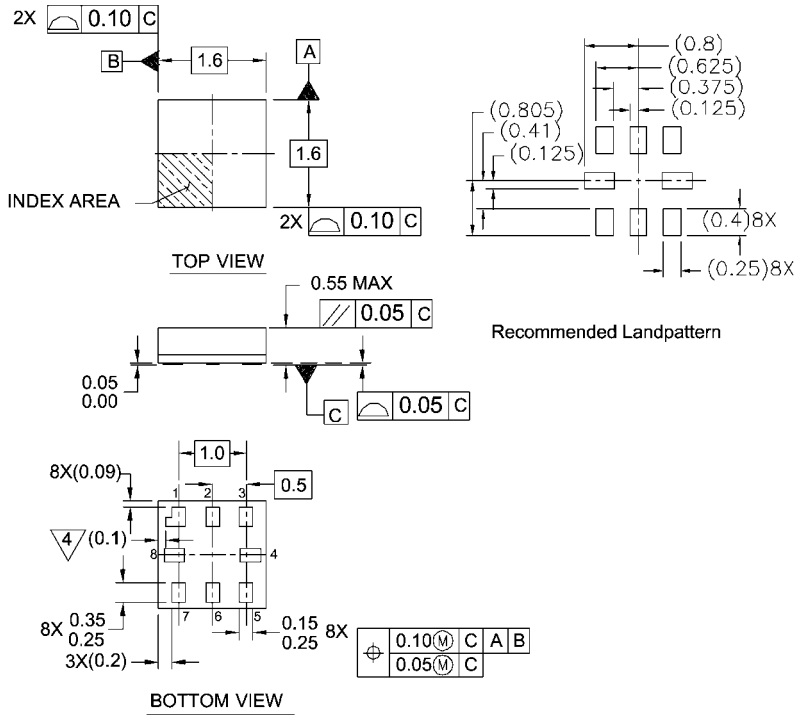
NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-187
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MAB08AREVC

**8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide**
**Package Number MAB08A**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




Notes:

1. PACKAGE CONFORMS TO JEDEC MO-255 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y.14M-1994
4. PIN 1 FLAG, END OF PACKAGE OFFSET.

MAC08AREVC

**Pb-Free 8-Lead MicroPak, 1.6 mm Wide**
**Package Number MAC08A**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

**LIFE SUPPORT POLICY**

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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